IN THE CLAIMS

No amendments have been made by the present response. A listing of all claims and status indicators is set forth below.

1. (previously presented) A method of processing a read request comprising the acts of:

transmitting a first read request from a requesting device, the first read request comprising a first system address;

receiving the first read request at a memory controller;

mapping the first system address into a first memory address, the first memory address comprising a first chip select, a first bank address, a first row address and a first column address; and

sorting the first read request by one of the first chip select and the first bank address such that the first read request is injected into a selected one of a first read queue and a second read queue based on the sorting by the one of the first ship select and the first bank address.

2. (previously presented) The method of processing a read request, as set forth in claim 1, comprising the acts of:

receiving a second read request at the memory controller, the second read request having a second system address and being received immediately subsequent to the first read request;

mapping the second system address into a second memory address, the second memory address comprising a second chip select, a second

bank address, a second row address and a second column address; and

sorting the second read request by one of the corresponding second chip select and second bank address such that the second read request is injected into the second read queue if the one of the first chip select and first bank address corresponding to the first read request is different as the one of the second chip select and second bank address corresponding to the second read request and wherein the second read queue is different from the first read queue.

3. (original) The method of processing a read request, as set forth in claim 2, comprising the act of alternately selecting read requests from the first read queue and the second read queue such that back-to-back requests are alternately processed between the first read queue and the second read queue.

4. (original) The method of processing a read request, as set forth in claim 3, wherein the act of alternately selecting read requests is performed by an arbiter.

5. (original) The method of processing a read request, as set forth in claim 2, comprising the act of selecting read requests to be processed such that back-to-back requests are not processed to the same chip select.

6. (original) The method of processing a read request, as set forth in claim 2, comprising the act of selecting read requests to be processed such that back-to-back requests are not processed to the same bank address.

7. (original) The method of processing a read request, as set forth in claim 2, wherein the second chip select corresponding to the second read request identifies a corresponding dual inline memory module (DIMM) to which the second read request is directed.

8. (original) The method of processing a read request, as set forth in claim 2, wherein the second bank address corresponding to the second read request identifies a

corresponding bank in a corresponding dual inline memory module (DIMM) to which the second read request is directed.

9. (original) The method of processing a read request, as set forth in claim 1, wherein the first chip select corresponding to the first read request identifies a corresponding dual inline memory module (DIMM) to which the first read request is directed.

10. (original) The method of processing a read request, as set forth in claim 1, wherein the first bank address corresponding to the first read request identifies a corresponding bank in a corresponding dual inline memory module (DIMM) to which the first read request is directed.

11. (original) A method of processing read requests in a redundant memory system comprising the acts of:

(a) receiving a plurality of read requests at a memory controller, each read request having a corresponding chip select and bank address;

(b) inserting the plurality of read requests into one or more queues; and

(c) prioritizing the processing of the plurality of read requests such that back-to-back read requests are not directed to the same one of a corresponding chip select and a bank address.

12. (original) The method of processing read requests in a redundant memory system, as set forth in claim 11, wherein act (b) comprises the act of inserting the plurality of read requests into one of a first queue and a second queue.

13. (original) The method of processing read requests in a redundant memory system, as set forth in claim 12, wherein act (c) comprises the act of alternately selecting read requests from the first queue and the second queue such that back-to-back requests are alternately processed between the first queue and the second queue.

14. (original) The method of processing read requests in a redundant memory system, as set forth in claim 13, wherein the act of alternately selecting read requests is performed by an arbiter.

15. (original) The method of processing read requests in a redundant memory system, as set forth in claim 11, wherein the chip select identifies a corresponding dual inline memory module (DIMM) to which a corresponding one of the plurality of read requests is directed.

16. (original) The method of processing read requests in a redundant memory system, as set forth in claim 11, wherein the bank address identifies a corresponding bank in a corresponding dual inline memory module (DIMM) to which a corresponding one of the plurality of read requests is directed.

17. (original) A memory cartridge comprising:

a plurality of memory devices;

a memory controller operably coupled to the plurality of memory devices and configured to receive a plurality of read requests from a requesting device, each of the plurality of read requests comprising a chip select and a bank address, wherein the memory controller is further configured to sort the plurality of read requests by one of the corresponding chip select and bank address;

a first and second read queues each operably coupled to the memory controller and each configured to store the read requests sorted by the memory controller; and

an arbiter operably coupled to each of the first and second read queues and configured to select read requests stored in the queues such that consecutive read requests do not have the same one of the chip select and the bank address.

18. (original) The memory cartridge, as set forth in claim 17, wherein the plurality of memory devices comprises a plurality of synchronous dynamic random access memory (SDRAM) devices.

19. (original) The memory cartridge, as set forth in claim 17, wherein the arbiter is configured to select consecutive read requests alternately between the first and second read queues.